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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,865	09/18/2003	Min-Su Kim	5484-110	8456

20575 7590 10/03/2005

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,865	KIM, MIN-SU	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,424,011 to Assaderaghi et al. in view of U.S. Patent No. 5,767,549 to Chen et al.

Regarding claim 1, Assaderaghi discloses a SOI structure comprising: a silicon substrate (bottom 'Si' layer in figure 5a), a BOX layer disposed on an upper surface of the silicon substrate ('BOX' layer in figure 5a), and an SOI layer disposed on the upper surface of the BOX layer ('SOI' layer in figures 5a-5l); the SOI layer including active areas (all 'SOI' regions in figures 5a-5l); a STI (202) formed in the device isolation areas (figure 5a); a first gate line (left-most "n-gate" in figures 7b and 8b, or 3rd gate from the left in figures 5a-5l) disposed over a portion of the active area (source, drain, and channel regions in figures 5, 7b, 8b) and a portion of the STI (see figure 8b; STI surrounds active region), the active area formed along two sides of the gate line (active region is SOI region; see figures 5e, 7b); an insulation layer (211) disposed on an upper surface of the active area and an upper surface of the STI (figure 5f-5h); and an LIC (interconnection including plugs 212 and wiring 213 in 'SRAM cell) disposed in contact with the insulation layer, an upper surface of a second gate line (right-most 'n-gate' in figures 7b, 8b or

2nd from the left in figures 5), and the active area, the LIC including a conductive material (column 6, lines 1-6, 15-20).

Assaderaghi fails to disclose the usage of a field oxide film formed on the surface of a well, such that the lower portion of the well is in contact with the BOX layer, but rather discloses STI isolation layers.

Chen discloses that it is advantageous for multiple-FET SOI structures to have device isolation regions including field oxide layers (38) formed only on the surface of a well (20), such that the bottom of the well is in contact with the BOX layer (14; see column 1, lines 25-67; column 3, lines 20-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SOI structure of Assaderaghi, such that the STI structures in the device isolation region are replaced by field oxide layers provided in the surface of a well, wherein the bottom of the well contacts the BOX layer, as suggested by Chen. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide semiconductor well portions between the buried oxide layer and the field oxide layer, so that floating body effects, which result in lower device gain and kinks in drain current vs. gate voltage (see Chen, column 1, lines 25-50) can be prevented, while eliminating the area penalty and fabrication complexity required for separate body contacts for each device by connecting all of the body portions through the device isolation region (Chen, 20), thus requiring only a single body contact for multiple devices (see Chen, column 1, lines 50-67, column 3, lines 25-40).

Regarding claims 2 and 3, Assaderaghi discloses that the local interconnect comprises tungsten and/or copper (column 6, lines 1-6, 15-20).

3. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assaderaghi et al. in view of Chen et al. and U.S. Patent No. 5,026,666 to Hills et al.

Regarding claims 4 and 7, Assaderaghi discloses a semiconductor structure having at least two active regions ('SOI' regions in figures 5a-5l) and a device isolation region ('STI' regions in figures 5a-5l), comprising: a silicon substrate (bottom 'Si' layer in figure 5a), a BOX layer disposed in contact with the substrate ('BOX' layer in figure 5a), a semiconductor layer (SOI layers in figures 5a-5l) disposed in contact with the BOX layer ('SOI' layer in figures 5a-5l); the SOI layer only having thickness in the active regions (see figures 5a-5l); a STI (202) formed in the device isolation areas (figure 5a); a first gate line (left-most "n-gate" in figures 7b and 8b, or 3rd gate from the left in figures 5a-5l) disposed over a portion of the active area (source, drain, and channel regions in figures 5, 7b, 8b) and contacting the STI (see figure 8b; STI surrounds active region; hence, the gate is disposed over the STI at the 'top' and 'bottom' portions of the gate line in figure 8b), a second gate line (right-most 'n-gate' in figures 7b, 8b or 2nd from the left in figures 5) crossing over another one of the at least two active regions and in contact with the STI (see figures 5, 7b, 8b – each gate line crosses over a different active region as in figure 5, and over a STI region as in figure 8b), an insulation layer (211) disposed in contact with the STI and the gate lines (see figure 5b); and a conductive metal fill (212 and 213) disposed in contact with the insulation layer, an upper portion of the first gate line, and another of the active areas (see figure 5f; layer 212 contacts each active region and gate layer, and is enclosed by, and thus contacts the insulation layer).

Assaderaghi fails to disclose the usage of a field oxide film formed on the surface of a well, such that the lower portion of the well is in contact with the BOX layer, but rather discloses STI isolation layers. The gate spacer layers (conformal layers 210 disposed on the sidewall of the gate) can reasonably be considered to be part of the gate line or alternatively part of the insulation layer (since both are typically silicon oxide), thus allowing Assaderaghi to meet the limitation of the insulation layer contacting a lower or side portion of the first gate line. Hence, this limitation is considered to be met by the combination of Assaderaghi and Chen alone. For the sake of argument, however, Assaderaghi does not specifically teach that a gate spacer could be omitted, such that the insulation layer is in contact with either the side or lower portion of the first gate line.

Chen discloses that it is advantageous for multiple-FET SOI structures to have device isolation regions including field oxide layers (38) formed only on the surface of a well (20), such that the bottom of the well is in contact with the BOX layer (14; see column 1, lines 25-67; column 3, lines 20-35).

Hills discloses a structure including multiple MOSFETs with gate regions interconnected to active regions through overlying insulating layers in a manner similar to the inventions of Assaderaghi or Chen. Hills further discloses that gate sidewall spacers (129, 130) are purely optional and are used only to provide LDD source/drain structures (see column 2, lines 25-30). It is noted that the omission of the sidewall spacers in Hills would cause the overlying insulating layer (201) to directly contact the side or lower portions of the gate line (see figures 2-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SOI structure of Assaderaghi, such that the STI structures in the device

isolation region are replaced by field oxide layers provided in the surface of a well, wherein the bottom of the well contacts the BOX layer, as suggested by Chen, and such that the sidewall spacers are omitted, as suggested by Hills. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide semiconductor well portions between the buried oxide layer and the field oxide layer, so that floating body effects, which result in lower device gain and kinks in drain current vs. gate voltage (see Chen, column 1, lines 25-50) can be prevented, while eliminating the area penalty and fabrication complexity required for separate body contacts for each device by connecting all of the body portions through the device isolation region (Chen, 20), thus requiring only a single body contact for multiple devices (see Chen, column 1, lines 50-67, column 3, lines 25-40). A person skilled in the art would further have been motivated to omit the sidewall spacers, thus causing the gate side or lower portions to directly contact the insulating film, because gates having or lacking sidewall spacers are well-known and well established in the art. Since Hills further indicates that such structures are optional, purely based upon the desired doping profile of the source and drain regions (Hills, column 2, lines 25-30), it would be well within the purview of a person skilled in the art to alternatively retain or omit the gate sidewall spacers based on the desired source/drain doping profiles.

Regarding claims 2, 3, and 8, Assaderaghi discloses that the local interconnect comprises tungsten and/or copper (column 6, lines 1-6, 15-20).

Response to Arguments

4. Applicant's arguments filed 7/22/05 have been fully considered but they are not persuasive.

The Applicant first argues that the wells in Assaderaghi are in the active region, and that the isolation region includes shallow trench isolation (STI) structures, but not wells. The Examiner agrees with this characterization of Assaderaghi, and instead has relied upon the Chen reference to teach the feature of a well formed in the isolation region with a field oxide layer disposed thereon.

The Applicant then argues that Chen does not teach an isolation region including a well. The Examiner disagrees with this characterization of Chen, since the isolation region (20) includes a well (20; also see column 3, lines 5-67 – individual doping of region 20 is disclosed) and a field oxide layer (38) formed thereon. Since Chen further provides motivations to use such a feature rather than using a completely isolated structure (like Assaderaghi) such as decreased floating body effects or required body contacts, as explained supra, the Examiner maintains that the invention as claimed is obvious over a combination of Assaderaghi and Chen.

The Applicant further notes that the isolation layer does not directly contact the side or lower portion of the gate as claimed in amended claim 4 and new claim 7. The Examiner notes that gate sidewall spacers are a ubiquitous feature in MOSFET transistor design and can thus be considered to be part of the 'gate line'. Furthemore, as the sidewall spacers are commonly formed of a silicon oxide, and the isolation layer is formed of a silicon oxide, the sidewall spacer and isolation layer can be considered to be part of the same layer, as there is no clear

differentiation between the layers once formed. Nevertheless, the Hills (US 5,026,666) reference has been added to address these new limitations.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

LAURA M. SCHILLINGER
PRIMARY EXAMINER